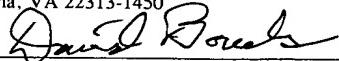


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PATENT

091-0215 (03-1119)

TRAVELING WAVE, MULTIPLYING D/A CONVERTER

BACKGROUND OF THE INVENTION

- 5 **[001]** The present invention generally relates to synthesis of high bandwidth, digitally modulated waveforms at microwave and millimeter wave frequencies and, more particularly, to a multiplying digital-to-analog converter (DAC) that exploits techniques of distributed amplification, also referred to as traveling wave amplification, to synthesize high resolution radio frequency (RF) signals at
- 10 microwave and millimeter wave frequencies and above without mixer up-conversion, and with a clock rate that can be much lower than the RF output frequency.
- 15 **[002]** While conventional superheterodyne architectures (e.g., a transceiver that uses a local oscillator to up-convert a baseband signal for modulation of an
- 20 RF carrier) have yielded excellent performance in a wide range of RF transceivers, the power consumption, size, and cost of such systems have often been limiting factors in their design and deployment. An often cited "holy grail" for RF transceivers is to incorporate a single element which accepts digital data as an input and directly produces a modulated RF output for transmission via an
- 25 antenna. Although a number of "bits-to-RF" direct synthesis approaches have previously been implemented, these techniques have not been able to reach microwave or millimeter wave frequencies with the resolutions, bandwidths, and tuning characteristics that are all simultaneously needed in broadband communications systems.
- 30 **[003]** For example, U.S. Patent No. 5,128,674 to Kong et al., incorporated

herein by reference, discloses essentially a single quadrant multiplying design with current level shifting circuits at the input and output which allow two quadrants (in the current-voltage plane) to be covered in an NPN-only design. The shifting operation will limit the bandwidth, and the impedance properties of 5 the single-ended design limit the achievable RF frequency and resolution (e.g., number of bits in a data word). U.S. Patent No. 5,134,400 to Hash, incorporated herein by reference, corrects the impedance properties to support microwave frequency operation, but relies upon high electron mobility transistor (HEMT) or metal Schottky field effect transistor (MESFET) switches and R-2R 10 resistor ladders. Requiring a HEMT or MESFET technology will limit the attainable resolution, and the RC (resistance-capacitance) time constants associated with resistor ladders inhibit the realizable data rates (e.g., adversely affecting bandwidth). U.S. Patent No. 5,394,122 to Conway et al., incorporated 15 herein by reference, makes use of power splitters, power combiners, RF switches, and a programmable attenuator and does not comprise a solution that can be integrated to support increasingly higher resolutions (for example, resolutions increasing beyond three bits and more) or higher data rates (e.g., 1.0 Giga-bits/second (Gbit/s) and greater).

[004] As can be seen, there is a need for a direct "bits-to-RF" digital-to-analog (D/A) conversion to support the synthesis of high bandwidth, digitally modulated waveforms at microwave and millimeter wave frequencies. There is also a need for the ability to support high resolution signals over a wide bandwidth at microwave and millimeter-wave frequencies with a clock rate that can be much lower than the output (RF) frequency.

25

SUMMARY OF THE INVENTION

[005] In one aspect of the present invention, a multiplying digital-to-analog converter includes a plurality of multiplying cells. Each multiplying cell is 30 connected to a differential local oscillator bias signal voltage. A digital input

includes a number of bits and each bit is connected to a binary-weighted number of the multiplying cells. An output connected to each of the plurality of multiplying cells provides a differential output current that is the product of the binary weighted value of the bits and differential local oscillator current.

- 5 **[006]** In another aspect of the present invention, a multiplying cell includes a local oscillator input that receives a continuous time local oscillator input signal. A digital input of the multiplying cell receives a single bit digital input signal, and a balanced output, having a constant output impedance, yields a differential output current signal, the differential output current signal being the multiplication of the continuous time local oscillator input signal by the single bit digital input.
- 10

- 15 **[007]** In still another aspect of the present invention, a multiplying cell includes a pair of current sources fed at a local oscillator input by a differential local oscillator bias signal voltage $V_{DC} \pm v_{LO}$ and which establish a differential local oscillator current i_{LO} superimposed on a DC (direct current) bias level I_{DC} . Two sets of current switches are connected to the current sources and have a digital input receiving an input signal comprising a bit having states H and L. The sets of current switches provide a differential output current signal I_{out} at a balanced cell output having an outl output and an outh output, so that:

- 20 $I_{out} = I_h - I_l$ where I_h is the output current at the outh output and I_l is the output current at the outl output; and I_{out} is a positive multiple of i_{LO} when the bit has state H and I_{out} is a negative multiple of i_{LO} when the bit has state L.

- 25 **[008]** In yet another aspect of the present invention, a traveling wave, multiplying digital-to-analog converter includes a local oscillator transmission line wherein the differential local oscillator bias signal voltage is provided on the local oscillator transmission line; an output transmission line; and a plurality of multiplying cells. Each of the plurality of multiplying cells is connected to the local oscillator transmission line and to the output transmission line. Each of the plurality of multiplying cells establishes a differential local oscillator current (i_{LO});
- 30 and propagation delays at each multiplying cell are matched between the local

oscillator transmission line and the output transmission line so that a plurality of output signals from each multiplying cell combine in phase on the output transmission line. A plurality of control lines provide a digital input including a plurality of bits wherein each bit is connected to the multiplying cells so that the

5 multiplying cells provide a differential output current on the output transmission line that is a product of a binary weighting of the plurality of bits and the differential local oscillator current (i_{LO}).

[009] In a yet further aspect of the present invention, a satellite transponder includes a traveling wave multiplying digital-to-analog converter having propagation-delay matched transmission lines and having an array of high and constant impedance multiplying cells for conversion of a high bandwidth digital input to a high frequency RF analog output. The array of high and constant impedance multiplying cells is connected along the transmission lines that propagate the high frequency RF analog output and along bit lines that

10 propagate the digital input.

15

[010] In a further aspect of the present invention, a method for digital-to-analog conversion includes steps of: feeding each of a plurality of multiplying cells a differential local oscillator bias signal voltage; providing a digital input including a plurality of bits; connecting each bit to a binary-weighted number of

20 multiplying cells of the plurality of multiplying cells; connecting an output to each of the plurality of multiplying cells; and providing a differential output current at the output.

[011] In a yet further aspect of the present invention, a method for direct bits-to-RF digital-to-analog conversion includes the steps of: propagating a local oscillator signal along an input transmission line; propagating a digital input signal along a plurality of bit control lines, the digital input signal comprising a plurality of bits, and the plurality of bits forming a digital word having a value b_n ; connecting a plurality of multiplying cells to the input transmission line and to an output transmission line, each of the plurality of multiplying cells establishing a

25 differential local oscillator current; and toggling the differential local oscillator

30

currents on the output transmission line using the multiplying cells so that a differential output current is the product of the value b_n and the differential local oscillator current.

[012] In another aspect of the present invention, a communication system 5 includes a traveling wave, multiplying digital-to-analog converter for conversion of a digital input to a high frequency analog output. The digital-to-analog converter has propagation-delay matched transmission lines. An array of constant high impedance, multiplying cells are connected along said transmission lines, at least one of which propagates the high frequency analog 10 output, and the array of multiplying cells are also connected along bit lines that propagate the digital input.

[013] There is a need in the art for RF transceivers with reduced power consumption, size, and cost that incorporate a single element which accepts 15 digital data as an input and directly produces a modulated RF output for transmission via an antenna at microwave and millimeter wave frequencies with the resolutions, bandwidths, and tuning characteristics that are all simultaneously needed in broadband communications systems. There is also a need in the art to provide such direct modulation at microwave and millimeter wave frequencies with significant reductions in the requirements for timing and 20 component matching.

[014] These and other features, aspects and advantages of the present invention will become better understood with reference to the following drawings, description and claims.

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BRIEF DESCRIPTION OF THE DRAWINGS

[015] Figure 1 is a schematic circuit diagram of a local oscillator (LO) current multiplying cell in accordance with one embodiment of the present invention;

[016] Figure 2 is a schematic circuit diagram of a unit-cell based multiplying 30 digital-to-analog (D/A) converter according to one embodiment of the present

invention;

[017] Figure 3 is a schematic circuit diagram of an LO current multiplying interpolation cell in accordance with one embodiment of the present invention;

[018] Figure 4 is a schematic circuit diagram of a unit-cell based traveling wave multiplying D/A converter according to one embodiment of the present invention;

[019] Figure 5 is a schematic circuit diagram of a mixed unit-cell/interpolation cell based traveling wave multiplying D/A converter according to another embodiment of the present invention;

[020] Figure 6 is a schematic circuit diagram of an interpolation-cell based traveling wave multiplying D/A converter according to another embodiment of the present invention; and

[021] Figure 7 is a flowchart diagram for a method for direct bits-to-RF digital-to-analog conversion according to one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[022] The following detailed description is of the best currently contemplated modes of carrying out the invention. The description is not to be taken in a limiting sense, but is made merely for the purpose of illustrating the general principles of the invention, since the scope of the invention is best defined by the appended claims.

[023] Broadly, one embodiment of the present invention provides a direct "bits-to-RF" digital-to-analog (D/A) converter architecture that supports the synthesis of high bandwidth, digitally modulated waveforms at microwave and millimeter-wave frequencies and above. Direct bits-to-RF D/A converters are useful in communication systems wherever data or synthesized signals are being transmitted - usually wirelessly - including, for example, satellites, television, cell phones, and wireless LAN, and any of these communication

systems may employ an embodiment of the present invention. In particular, transceivers incorporating an embodiment of the present invention may be used, for example, in communications satellites, where they may be effective at reducing commercial satellite payload cost and improving overall transceiver 5 performance by providing a direct bits-to-RF data converter. More specifically, such an RF D/A converter may be particularly valuable for communications satellite transponders.

[024] By architecting a D/A converter around a set of identical (e.g., component matched) multiplying unit cells having high and constant input and 10 output impedances, distributed amplifier (i.e., traveling wave) concepts can be applied to greatly extend the frequency and bandwidth that can be realized. While some embodiments of the present invention may provide D/A conversion at conventional frequencies and bandwidths, the architecture of some 15 embodiments may allow the RF output frequency to be scaled according to traveling wave concepts so that arbitrarily high frequencies and bandwidths can, in principle, be realized. For example, from a traveling wave point of view, the architecture of one embodiment provides a constant impedance structure, e.g., transmission lines connecting an array of identical cells, so that the impedance presented by the array is uniform along the length of the transmission lines, 20 enabling waves to travel along the structure without reflection or dissipation. Related but of secondary importance is that the architecture of one embodiment may also provide a structure whose impedance may be independent of frequency so that dispersion of a wave propagating along the structure may be limited. Employing such scalability, high bandwidth D/A conversion at 25 microwave to millimeter wave frequencies, exceeding that of the prior art, can, in practice, be realized. Furthermore, the distributed unit cell-based architecture can be arranged to leverage spatial averaging into significant reductions in the requirements for timing and component matching. These concepts, when used in conjunction with a multiplying D/A converter, allow high resolution signals to 30 be synthesized at higher RF output frequencies than achieved in the prior art,

for example, microwave and millimeter wave frequencies, without mixer up-conversion stages, and with a clock rate that can be much lower than the RF output frequency.

[025] Embodiments of the present invention provide a traveling wave multiplying D/A architecture that addresses and overcomes limitations in the prior art by:

- 5 1) Decoupling the output frequency from the clock rate (e.g., the clock rate of the digital input signal), thereby permitting very high frequencies to be synthesized while maintaining the resolution and linearity commensurate with
- 10 the bandwidth of the signal;
- 15 2) Developing a constant impedance traveling wave structure to support microwave and millimeter wave output frequencies;
- 3) Utilizing a unit cell-based D/A core to alleviate the matching requirements needed to achieve a given resolution; and
- 4) Providing an impedance-matched, self-decoding data bus, i.e., bit control lines, to yield very high data rates.

[026] Furthermore, in many applications, an embodiment's ability to support a high resolution over a wide bandwidth can obviate the need to build a tunable transmitter. For example, different channels can be addressed merely by adjusting the input digital data stream through digital signal processing (DSP). In bringing all of these capabilities together in an approach that can be fully integrated into the communication system, the proposed architecture can provide a tremendous flexibility in the design of microwave and millimeter wave communication systems. In general, microwave and millimeter wave frequencies refer to frequencies greater than about 1.0 GHz, and such frequencies may correspond to electromagnetic waves having wavelengths, when radiating in free space, that are about 300 mm and shorter. (In guided wave media, the corresponding wavelengths may be considerably shorter.)

[027] Referring now to Figure 1, an exemplary circuit diagram for a local oscillator (LO) current multiplying "unit cell" 100 is shown in accordance with

one embodiment. To be able to realize a traveling wave, multiplying D/A converter, a "unit cell" circuit - such as unit cell 100 - may be first needed as an element which provides for 1) the multiplication of a continuous-time LO input signal by a single bit digital input, and 2) constant (and large-valued, e.g., 5 $1,000\Omega$ (ohms) and greater) input and output impedances. Figure 1 illustrates one example circuit of a unit cell 100 having these properties. Unit cell 100, for example, may be topologically similar to a doubly-balanced active mixer. In other words, the interconnections of components, such as current sources and switches, and circuit routing of signals, such as input signals and output signals, 10 may be similar. The current sources 102 (Q1-Q2) may establish a differential LO current 104 ($\pm i_{LO}$) superimposed on a DC bias level (I_{DC}). For example, current sources 102 may be fed a differential LO bias signal voltage 103 ($V_{DC} \pm v_{LO}$). Two sets of current switches 106, 108 (Q3-Q4, Q5-Q6) toggle the direction of 15 these LO currents 104 as applied to the balanced unit cell output 110 (output current I_h at outh, output current I_l at outl) based on the state of the digital input 112 (labeled "bit" in Figure 1). (Note that digital input 112 "bit" connected at Q6 is the same as "bit" connected at Q3 - the connecting line is not shown to simplify the drawing. Also, note that "(bit)^c" is the inverse, or complement, of "bit", i.e., (bit)^c is L when bit is H and (bit)^c is H when bit is L.) The operation of 20 the multiplying unit cell 100 is summarized in Table 1. The differential output current signal 114 ($I_{out} = I_h - I_l$) is $+2i_{LO}$ when bit is high (H) and $-2i_{LO}$ when bit is low (L), thus yielding an output signal (e.g., differential output current signal 114) having only a component at the applied LO frequency.

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Table 1: Logic Table for the LO Current Multiplying Unit Cell

<u>bit</u>	<u>I_h</u>	<u>I_l</u>	<u>$I_{out} = I_h - I_l$</u>
H	$I_{DC} + i_{LO}$	$I_{DC} - i_{LO}$	$+2i_{LO}$
L	$I_{DC} - i_{LO}$	$I_{DC} + i_{LO}$	$-2i_{LO}$

[028] The constant, i.e., state independent, output impedance and bias current properties of the multiplying unit cell 100 allow a multi-bit (e.g. N-bit) multiplying D/A converter to be realized by ganging together $2^N - 1$ copies of the unit cell and connecting the appropriate binary-weighted number of cells to each digital input. For example, Figure 2 illustrates a multi-bit multiplying D/A converter 200 with $N = 3$, according to one embodiment. To simplify the drawings, digital input 112 signals are shown single-ended, i.e., the inverse (bit)^c of each bit is not shown. Note that input bit₂ may be connected to four unit cells 100, bit₁ may be connected to two unit cells 100, and bit₀ may be connected to one unit cell 100 so that the weights for digital inputs 112, bit₂, bit₁, and bit₀, may be respectively 4, 2, and 1.

[029] Still referring to Figure 2, unit cell outputs 110, connected to output 210 of D/A converter 200, may be biased by load resistors 216, which may have any value that provides an appropriate load impedance. For example, the size of the load resistors 216 may be constrained by various factors including power supply headroom, power dissipation, and transistor breakdown. Driving each unit cell 100 with the same LO/bias signal voltage 103, the unit cell outputs 110 may be connected to yield a differential output current 214 (i_{out}) given by the following formula:

20 $i_{out} = 2(bit_2 2^2 + bit_1 2^1 + bit_0 2^0) i_{LO}$ (1)

where the expression in parentheses is the value of the input digital word, hereafter referred to as b_n . Stated more generally, the output current 214 (i_{out}) from the multiplying D/A converter 200 can be recognized as the product of b_n and the LO signal (i_{LO}). (The factor of 2 arises from the fully differential current sources where the amplitude of each side is taken as i_{LO} .) Equivalently, the digital input can be viewed as modulating the envelope of the LO by setting its amplitude from bit time to bit time (as determined, for example, by the clock rate), effectively up-converting the digital data about the LO.

[030] As seen in Figure 2, while the multiplying D/A converter 200 may comprise logical groupings of unit cells 100 (according to which bit of b_n the unit

cells are connected to), the arrangement of each logical grouping need not be comprised of physically adjacent cells 100. Basing an architecture upon identical unit cells provides a flexibility to construct patterns in the groupings. One particularly useful arrangement may be to interleave the bit positions,
5 thereby effecting a "spatial averaging" across the array 202 of unit cells 100. By making the most significant bit (MSB) consist of every other cell 100 throughout the array 202, and then filling the gaps from the outside toward the middle with the remaining bits (starting with the next most significant bit) linear gradients across the array 202 may be averaged out in the summation which forms the
10 output current 214. Such gradients may result, for example, from process, temperature or electrical limitations (e.g., attenuation) and may defeat the linearity of the D/A conversion at output 214 if not compensated for.

[031] Returning again to the 3-bit case shown in Figure 2, bit₂ (the MSB) may connect to every other unit cell 100 (as shown) while bit₀ (the least
15 significant bit, LSB) may connect to a single unit cell 100 at the center of the array 202 and bit₁ (the next most significant bit) may connect to the remaining cells 100. Consider, for example, an attenuation of the LO/bias signal 103 from left to right across the array 202 such that the amplitude of the LO current decreases by a factor δ from one unit cell 100 to the adjacent unit cell 100. If
20 the first cell flows $\pm (1+3\delta) i_{LO}$, the second $\pm (1+2\delta) i_{LO}$, and so on, the middle cell in the array 202 will flow $\pm i_{LO}$, and the last will see $\pm (1-3\delta) i_{LO}$. Thus, the output from the LSB bit₀ will be $\pm i_{LO}$, bit₁ will provide $\pm [(1+2\delta) + (1-2\delta)] i_{LO} = \pm 2 i_{LO}$, and the MSB bit₂ will similarly sum to $\pm 4 i_{LO}$. Linearity in the D/A conversion may therefore be maintained in the presence of any linear gradient across the
25 array 202 of unit cells 100, including those gradients which may result from device or timing mismatches.

[032] By extending the above-described techniques using more unit cells, a multiplying D/A converter of arbitrary resolution, i.e., N-bit, where N may be any positive integral value, may - in principle - be realized. However, for converter

resolutions beyond about 8-9 bits, the power consumption and die area needed for an array of $2^N - 1$ unit cells may become prohibitive. An alternative approach for extending the resolution is to incorporate bits that may interpolate between successive states of the unit cell array.

- 5 [033] One means of implementing an interpolation bit may be to affix a resistive attenuator 320 to the LO input 303 of a multiplying unit cell 100 to provide a multiplying interpolation cell 300, as shown in Figure 3. As the differential bias LO feed lines (not shown in Figure 3) connected to LO input 303 are at the same DC potential, no DC current (neglecting base currents) may
- 10 flow in the attenuator 320 and the current sources 302 (Q1-Q2) may have the same bias (I_{DC}) as in the unit cells 100. However, provided that the current sources 302 (Q1-Q2) function as linear transconductors, the $\pm v_{LO}/2$ furnished by an attenuator 320 with four equal-valued resistors 322 may result in the current sources 302 (Q1-Q2) establishing a differential LO current 304 ($\pm i_{LO}/2$) superimposed on a DC bias level (I_{DC}). Thus, a differential output current signal 314 ($I_{out} = I_h - I_l$) may be $\pm i_{LO}$ (bit_n), which may be half the output of a unit cell 100 in the array 202. Of further significance is that this interpolation may be achieved with a circuit (e.g., multiplying interpolation cell 300) having the same output impedance properties and the same input signals - differential LO bias
- 15 signal voltage 103 - as the unit cell 100. These features may allow the interpolation cells 300 to be incorporated into the unit cell 100 array 202, while maintaining all of the advantages of component matching and spatial averaging afforded by the unit cell approach.

- 20 [034] Additional interpolation bits, i.e., additional levels for differential output current signal 314 (I_{out}), may be obtained simply by tapping the resistive attenuator 320 in different locations (e.g. to get $I_{DC} \pm i_{LO}/4$, $I_{DC} \pm i_{LO}/8$, etc.) The additional differential output levels may be similar to the binary weights for digital inputs 112 as described above, and example output level weights are indicated by numerals on interpolation cells 300 shown in Figures 5 and 6. It
- 25 30 should be noted that the additional output levels may be realized without

employing an R-2R ladder to split or combine LO/RF signals, allowing multiple bits of interpolation to be realized in a high frequency, high bandwidth data converter. Using m interpolation bits - or interpolation cells 300 - may reduce the number of total number of cells in an N -bit multiplying D/A to:

$$5 \quad (2^{N-m} - 1) + m. \quad (2)$$

[035] Conceivably, then a multiplying D/A converter could be achieved with just $m = N$ interpolation bits or interpolation cells 300. For example, Figure 6 illustrates a multiplying D/A converter 600 for the case $m = N = 3$, which may use just three interpolation cells 300 to provide the same 3-bit resolution provided by seven unit-cell multiplying D/A converter 200 shown in Figure 2. Most designs, however, may benefit from some mixture of unit cells 100 and interpolation cells 300. For example, Figure 5 illustrates a multiplying D/A converter 500 for the case $N = 3$ and $m = 1$, which may use four cells to provide the same 3-bit resolution provided by seven unit-cell multiplying D/A converter 200 shown in Figure 2. In these two figures, the weights for digital inputs 112, as described above, are indicated by the number on each multiplying cell 100 or 300.

[036] Exemplary traveling wave multiplying D/A converters 400, 500, 600 are shown in Figures 4, 5, and 6 according to various embodiments. As seen in Figure 4, for example, multiplying unit cells 100 may be arrayed along input (LO) transmission line 430 and output transmission line 440. Considering now that the multiplying unit cells 100 (and interpolation cells 300) have high (and constant) input and output impedances, the cells may be arrayed along input and output transmission lines 430, 440 without appreciably impacting the signals traveling on those lines. Furthermore, any capacitances at the inputs and outputs of the unit cells can be absorbed into the characteristic impedances Z_0 of the transmission lines 430, 440, allowing very high frequencies to be handled by the D/A core of the architecture (e.g. D/A converter 400). For example, the architecture allows the frequencies to be scaled, as described above, to accommodate microwave and millimeter wave frequencies and

higher.

[037] Such an arrangement of multiplying cells 100, 300 arrayed along input and output transmission lines 430, 440, as depicted in Figures 4, 5, and 6, may be similar to that of a distributed amplifier. Provided that the LO transmission lines 430 and output transmission lines 440 have the same propagation velocities, the output signals 114 from each unit (interpolation) multiplying cell 100 will combine in phase - producing output signal 214 - as each LO to output path (e.g., a path from LO transmission line) will see the same overall delay. The condition for matched velocities is that the product of the inductance and capacitance per unit length of the loaded transmission lines 430, 440 (i.e., including the input and output capacitances from the unit cell 100 at each tap point) must match between the LO lines 430 and the output lines 440. Alternatively, if the propagation velocities could not be matched, the transmission line on one side could be made slightly longer than the other to equalize the delay from cell to cell, as apparent to one of ordinary skill in the art. Additionally, a variety of options are known in the art for matching propagation delays in distributed amplifiers, which may be applied to embodiments of the traveling wave data converter of the present invention.

[038] Nominally, the delays along the control (or bit) lines 450 must also match - both each other and the delays along the LO and output transmission lines 430 and 440. Distributing dummy loading (as known in the art) along the control lines 450 can equalize the number of capacitive loads driven by each digital input 112 signal, allowing the velocities to match for the digital input 112 signals (in spite of the different number of multiplying cells driven by each bit line 450). However, a constant error in velocity along a control line 450 may represent a linear error term in the delay along the array 202, and may thus be compensated through the spatial averaging achieved by interleaving (described above). Very high data rates for digital input 112 signals can thus be achieved. For example, bit rates exceeding 1.0 Gbit/s for digital input bits 112 may be realized. The interleaved unit cell architecture proposed here thus provides

improved data converter linearity in the presence of dynamic errors as well as static errors.

[039] Applying traveling wave concepts to the multiplying D/A approach greatly extends the bandwidth, output frequency, and resolution that can be 5 achieved with a data converter - such as data converters 400, 500, 600. This combination of extended bandwidth, output frequency, and resolution can be enabled by the realization of multiplying circuits (unit cells 100 and interpolation cells 300) having constant and high valued terminal impedances. For example, the terminal impedances of the multiplying circuits (e.g., cells 100, 300) should 10 be much greater (e.g., by a factor of 10 or more) than the characteristic impedance, Z_0 , of the transmission lines 430 and 440. As for the output impedance of the traveling wave D/A converters 400, 500, 600, the output impedance of the converter 400, for example, should match the characteristic impedance of the output transmission lines 440. For example, a matching 15 output impedance to a typical characteristic impedance of the output transmission lines may have a value in the neighborhood of 30Ω .

[040] By constructing an embodiment - such as converter 200 or converters 400, 500, or 600 - of identical multiplying cells - such as unit cells 100 or interpolation cells 300 or combinations of both - good component matching 20 (e.g., of transistor properties and resistor values) as well as matching of propagation delays, may be achieved. In addition, by constructing an embodiment of an array of identical multiplying cells to improve component matching and matching of propagation delays, and by spatially averaging across the array, for example, by interleaving the connections of the multiplying 25 cells on the bit control lines (as described above) to cancel linear gradients that may result, for example, from process, temperature or electrical limitations (e.g., attenuation), linearity in the D/A conversion may be preserved. Collectively, the features disclosed here may yield a significant advance in the resolution, bandwidth, and tuning characteristics of direct bits-to-RF converters - such as

converters 400, 500, 600 - which may operate at microwave and millimeter wave frequencies and above, while being amenable to the requirements of integration and low power consumption.

[041] Figure 7 illustrates a method 700 for direct bits-to-RF digital-to-analog conversion. At step 702, a local oscillator signal - such as differential LO bias signal voltage 103 - may be propagated along an input transmission line - such as input transmission line 430. Also, a digital input signal - such as digital input 112 - may be propagated, at step 704, along a bit control line - such as bit control lines 450. At step 706, the input transmission line 430 and output transmission line 440 may be connected through a plurality of multiplying cells - such as unit cells 100 or interpolation cells 300 - which may establish a differential LO current 104 ($\pm i_{LO}$). The multiplying cells may be connected so that propagation delays are matched and so that signals propagating along the transmission lines may combine in phase, enabling high bandwidth data conversion at high frequencies, for example, at microwave and millimeter wave frequencies and above. Furthermore, either a binary-weighted number of multiplying unit cells 100, or an interpolation cell 300 providing the appropriate binary weighted interpolation bit, may be connected at each bit control line so that, at step 708, toggling the differential LO currents on the output transmission line using the multiplying cells may produce a differential output current that may be the product of the value of the weighted binary bits of digital input 112 and the differential LO current 104.

[042] It should be understood, of course, that the foregoing relates to preferred embodiments of the invention and that modifications may be made without departing from the spirit and scope of the invention as set forth in the following claims.